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Improved cycling stability of silicon thin film electrodes through patterning for high energy density lithium batteries

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ABSTRACT

The mechanical degradation of electrodes caused by lithiation and delithiation is one of the main factors responsible for the short cycle life of lithium-based batteries employing high capacity electrodes. In this report, we introduced a simple patterning approach to improve the cycling stability of silicon electrode, which is considered as the next generation negative electrode due to its high Coulombic capacity and low cost, but is limited by the mechanical degradation associated with large volume variations during cycling. The pattern design is based on the observation of a critical size for the crack gap in continuous films. An improvement in cycle life was noted when the pattern size was below the critical (7–10 μm) size, in which case the Si electrode patches adhered well to the Cu substrate after many cycles. By taking the plastic deformation in both Si thin film and substrate into consideration, the calculated crack spacing is consistent with experimental observations. Theoretical considerations gave a feasible explanation for the failure of Si pattern above the critical size. These results suggest a new approach to extend the cycle life of Si-based electrode materials using size to control and relax the stress due to lithiation and delithiation.

1. Introduction

Silicon (Si) has been considered as an alternative to commercial graphite as the negative electrode in lithium ion batteries to provide much higher specific capacity (4200 mAh g^{-1} for Si in the form of $Li_{22}Si_5$ as compared with 372 mAh g^{-1} for fully lithiated graphite, LiC_6). However, the volume change of up to 300 vol.% for Si during the lithium lithiation (insertion) and delithiation (extraction) processes leads to fracture of the active Si materials and/or loss of electrical contact with the conductive additives or the current collectors [1]. The fracture of Si normally creates new surfaces, which results in the formation of a new solid electrolyte interphase that consumes more lithium irreversibly, leading to capacity degradation [2,3]. Different approaches have been proposed to extend the cycle life of Si-based electrodes, including pure micro- and nano-scaled Si powder dispersed in an inactive matrix, Si nanowires, or Tin (Sn) thin films, as summarized by Kasavajjula et al. [4].

The electrochemical lithiation of crystalline Si has been proved to be complicated, and does not follow the thermodynamic phase diagram at room temperature [5]. The insertion of lithium ion into the Si lattice eventually destroys the crystal structure and leads to an amorphous transformation of the Si. At the end of discharge (around 30–50 mV vs. Li [6]), the Li–Si phase undergoes an abrupt crystallization transformation to form $Li_{15}Si_4$, which does not exist in the equilibrium phase diagram. Therefore, the theoretical specific capacity of 4200 mAh g^{-1} has not been observed electrochemically, and the maximum value of 3579 mAh g^{-1} observed corresponds to a composition of $Li_{15}Si_4$ [7]. There have been suggestions that the change in structure from amorphous Si to crystalline $Li_{15}Si_4$ creates a phase boundary with abrupt mechanical property variation, which leads to the generation of microcracks and other defects. Several approaches have been proposed to prevent the failure induced by this phase transformation. One is to set the cutoff voltage to be greater than 50 mV for discharge to avoid the formation of $Li_{15}Si_4$ [5], at the cost of losing capacity at low potential. Another approach is to decrease the physical size of the Si electrode based on the experimental observation that the phase transition to crystalline $Li_{15}Si_4$ did not occur for Si sizes below 2 μm [4]. Although the reason for this phenomenon remains unclear, a possible explanation is that the physical constraints from the attached substrate could be responsible for preventing the phase transformation. On the other hand, the effect of feature size can also be explained by Graetz's work [8], which showed that amorphous Si thin films ~100 nm thick possessed better properties as this was

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below the critical crack size given by:

$$a_c = \frac{2}{\pi}\frac{K_{1c}^2}{\sigma^2} \quad (1)$$

where the fracture toughness, K_{1c} and yield strength σ in polycrystalline silicon are approximately 0.751 MPa $m^{-1/2}$ and 1.1 GPa, respectively, which yield a critical flaw size of around 300 nm. Several Si film electrode studies have been published subsequently that are motivated by this mechanical stability argument, including the roughening of the current collector to improve mechanical adherence of Si films during cycling [9–11].

Based on the work mentioned above, it is clear that the proper design of the Si microstructure may sufficiently alleviate mechanical degradation and extend the cycle life of Si-based electrodes. In this work, we designed a series of experiments to further understand the fracture of Si thin film electrodes. We chose the film thickness around 100 nm in order to retain the coating adhesion to the current collector. We first deposited amorphous Si thin films on a copper current collector and, based on its characteristic fracture behavior, designed a Si pattern that would not be as prone to form microcracks, thereby improving cycling stability. We also provide some preliminary theoretical considerations to explain the unique fracture behaviors related with size effect.

2. Experimental

Both continuous and patterned Si thin films were deposited onto Cu plate substrates by electron beam evaporation (Thermionics) using 99.999% pure Si pallets as the starting material. Si films with thickness of 100 nm were deposited on to 0.5 mm thick Cu substrates at room temperature using a base pressure less than 1.0×10^{-8} Torr in order to avoid oxidization. The surface copper oxide was etched from the copper substrate with 5% HCl prior to being placed inside the deposition chamber. A Si deposition rate of 0.2 nm s^{-} was used (deviation typically less than 0.02 nm s^{-}), and the thickness of the film was controlled with a quartz crystal monitor (Inficon). A Ni mesh was mounted as the mask (over the current collector substrate) and held in firm contact with the surface to grow the patterned Si films. Three kinds of meshes were employed: 500 (with hole size of 7.6 μm × 7.6 μm), 1000 (18 μm × 18 μm) and 2000 (39 μm × 39 μm). Similar approaches for making patterned thin film electrodes can also be found in the work of Dahn et al. [1,12].

The continuous Si thin film was used as the working electrode and was tested in the form of coin cell. Lithium was used as the counter electrode. The electrode was cycled with a constant current of about 0.1 mA with a cutoff discharge voltage of 100 mV vs. Li. The electrolyte was 1 M LiPF6 in 1:1 (v/v) of ethylene carbonate (EC) and dimethylcarbonate (DMC).

Patterned Si samples were used directly as the working electrode in a three-electrode electrochemical beaker cell with lithium metal as both the counter and the reference electrodes. The electrode was first discharged at a constant current to 0.5 V and charged to 1.2 V for 5 cycles. This sequence was repeated with the voltage at the end of discharge lowered to 0.4, 0.3, 0.2, 0.1, and 0.01 V, respectively. The current densities for 500, 1000, 2000 mesh samples were 15.8, 39.5, and 63.2 μA cm^{-2}, respectively. The same electrolyte was the same as that used for the continuous Si thin film.

The tested (delithiated) samples were washed with diethyl carbonate (DEC) to remove the extra $LiPF_6$ on the Si film surface, and the surface morphology and composition were examined with an FE-SEM coupled with EDX. The depth profile of composition on the tested samples was measured by X-ray photon spectroscopy (XPS). The nanoindentation was carried out on Hysitron TI900 with load control capability, and the hardness and modulus of the Si pattern and Cu was calculated from the loading and unloading curves.

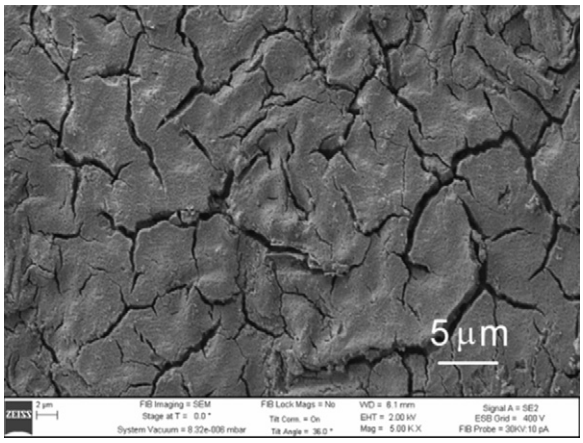

Fig. 1. The surface morphology of Si thin film after testing for 12 cycles.

3. Experimental observation

3.1. Continuous Si thin films

Fig. 1 shows the surface morphology of a continuous Si thin film after 12 cycles. Many randomly aligned microcracks have been generated in the thin film due to the volume change induced by the lithiation and delithiation process. The cracking shown in Fig. 1 is typical of fractures that occur under tension [13], and is similar to that observed experimentally in the literature [14] for Si thin films deposited on Cu current collectors. These cracks, that occur under tension, normally lead to stress relaxation [15], which prevents film delamination from the substrate. Compressive stresses, on the other hand, generally lead to buckling and delamination as well of the thin films.

The insertion of lithium into the Si thin film causes a volume expansion, but it is the constraint from the Cu substrate that puts the Si under compression. The Cu substrate, on the other hand, is subjected to tension, and will deform plastically when the generated tensile stress becomes greater than its yield strength. The presence of crumpling of the substrate in some areas after several testing cycles, and an increase in hardness of the Cu (as will be shown later), confirms that this indeed occurs in the Cu. However, when Li is delithiated from the Si thin film, the residual plastic deformation will induce a tensile stress in the Si film instead. This tensile stress, coupled with the fact that the delithiation process has already damaged the bond network in the amorphous Si thin film, will lower the strength of the film and cause the formation of microcracks. These microcracks will be random since the amorphous Si is isotropic, and there is no preferential direction for the microcrack to follow.

Generally, phase boundaries induced by phase transformation cause fracture of the silicon electrode. However, no phase transformation was allowed since the 100 mV cutoff voltage is above that which leads to transformation of the amorphous state to crystalline $Li_{15}Si_4$. (The higher cutoff voltage also limits the initial capacity to about 1600 mAh g^{-1}, as shown in Fig. 2, which is lower than the theoretical capacity.) The microcracks were, therefore, most likely due to cycling-induced fatigue. The density of microcracks, or the spacing between cracks depends on the mechanical properties of both the coating and the substrate as described below. The capacity gradually reduced after the first cycle due to the formation of the microcracks and the formation of an SEI layer on the fresh fracture surfaces, consistent with our introductory discussion above.

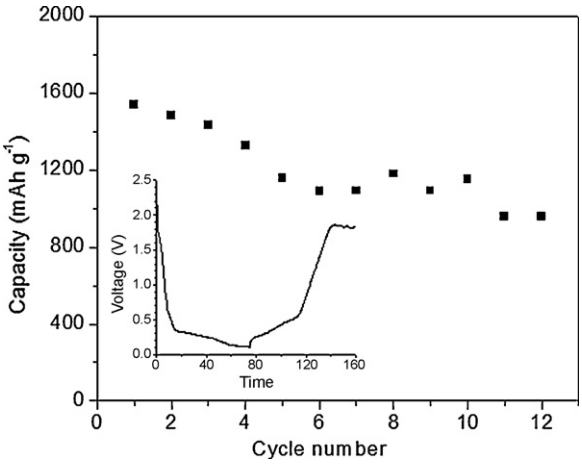

Fig. 2. Cycling behavior of continuous Si thin film electrode.

The formation of microcracks in the Si thin film is related to the energy release rate:

$$G = g(\alpha, \beta)\frac{\pi(1-\upsilon_f^2)\sigma_f^2 h}{2E_f} \quad (2)$$

where σ_f is the average stress in the film acting normal to the crack line before generating cracks, h is the film thickness, E_f is the effective modulus of elasticity and $g(\alpha, \beta)$ is a function of the Dundur's parameters characterizing the elastic mismatch between the film and the substrate. A detailed derivation of the equation can be found in Hutchinson and Suo [13]. Only when the strain energy release rate exceeds the fracture resistance can the crack propagate in the film, substrate, or along the interface. In our study, the channel-through cracks were generated under tension and no delamination occurred after 12 cycles. Therefore, we can apply Mode I fracture resistance to the thin film. Obviously, the thicker the film, the higher the strain energy release rate, and the more probable that the film will fracture. This is consistent with the better cyclability of the films with nanoscale thickness [5].

Based on Eq. (1), if the characteristic length is less than 300 nm, no microcrack will be generated. However, in our case, we found that the channel-through cracks formed a network with a characteristic length of about 10 μm. The possible reason to cause the difference is that Si has been considered as an elastic material throughout the cycling process in terms of our application of Eq. (1). However, the material properties change significantly during the lithiation/delithiation process: the modulus of lithiated silicon is much lower than pure Si (80 GPa for amorphous Si and 18 GPa for amorphous $Li_{15}Si_4$ [16]) and lithiated Si undergoes severe plastic flow when the stress level is above 1.4 GPa [17]. The energy to create new surface areas emanates from the strain energy induced by the lithium ion insertion. However, since a part of the strain energy is also consumed by generating plastic deformation in the copper substrate, it is difficult to correlate the strain energy released with the fractured surface area. We will explain this in details in Section 4.

3.2. Patterned Si thin films

Based on the observation in Fig. 1, we hypothesized that a proper design of the Si pattern with feature sizes below the critical size could avoid cracking. Dahn's group has published several papers on patterned electrode materials, and they applied the patterning approach to investigate the volume change during the cycling with atomic force microscope [1,12]. In this study, we utilized the gaps between Si patterns for relaxing the stress induced by the lithiation

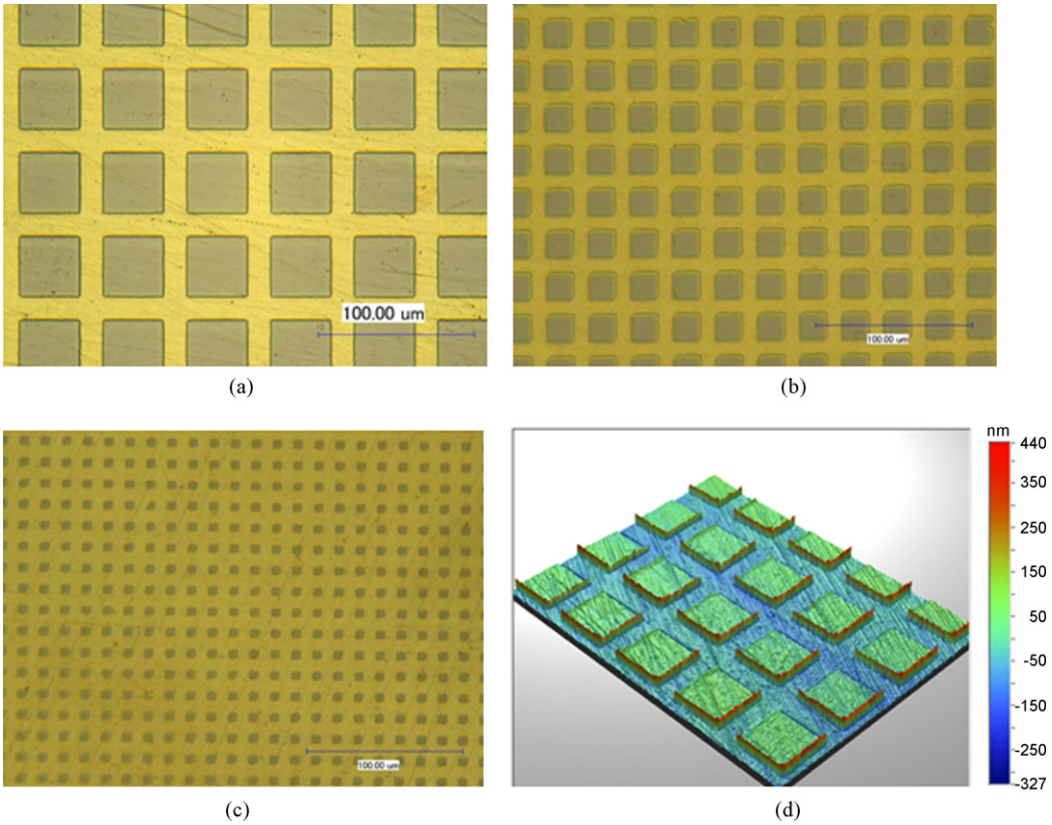

Fig. 3. Si patterns with different sizes (a) with 500 mesh, the pattern width is around 40 μm; (b) with 1000 mesh, the pattern width is around 17 μm; (c) with 2000 mesh, the pattern width is around 7 μm; (d) the 3D profile of the patterns.

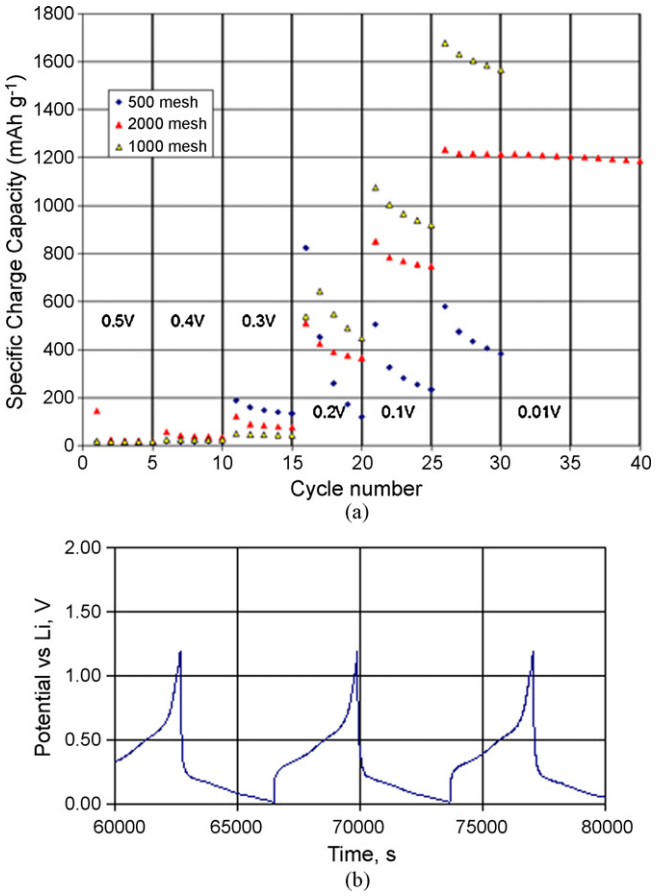

Fig. 4. Cycling test of Si patterns with different sizes. (a) Capacity retention as a function of cycle number. (b) Typical charge–discharge profiles during cycling.

and delithiation process to alleviate the mechanical degradation. Since the crack spacing is around 7 μm as shown in Fig. 1, we designed the pattern size to vary from 40 μm down to 7 μm. Fig. 3 shows the as-deposited Si patterns with different sizes on the copper current collector. The first 3 images in Fig. 3 were taken at the same magnification. The irregular feature with the smallest pattern size is due to mask defects and the shadow effect of the mask during deposition.

In order to obtain a robust correlation between the pattern geometry and the cycling behavior, we first cycled all the samples with gradually decreasing cutoff voltages to condition the samples. Then we set the cutoff voltage to below 0.01 V in order to generate higher strain than that used in previous case of a continuous film. Fig. 4 shows the electrochemical cycling test results from the pattern with different sizes. Samples with smaller patterns showed higher stability and capacity retention. For the samples with larger patterns, the capacity sharply dropped to zero at a cutoff voltage of around 0.01 V. The morphologies of the samples with different patterns are shown in Figs. 5–7. Si coatings with a 40 μm pattern (500 mesh) were completely peeled off, as shown in Fig. 5. Only the image contrast indicated the pattern location, and the EDX analysis did not detect any Si signal from the pattern. Instead, strong signals of F and C were detected, which could be from the SEI layer formed on the Cu substrate after the Si thin film was peeled off from the pattern.

For the 17 μm pattern (1000 mesh), a portion of the patterned coating peeled off, and no channeling cracks were observed on the remained Si patterns. Some buckling was observed due to the compressive stress and the weak interface. The EDX on the Si pattern shows strong Si peaks, and the F, C and O peaks detected are from the SEI layers.

For the sample with width smaller than the typical crack spacing in continuous films (7 μm pattern using 2000 mesh mask), the Si patterns all remained on the Cu substrate, as supported by the EDX results. The integration of the Si patterns with smaller sized features on the Cu substrate gives rise to better cycling stability and capacity retention. Clearly, by choosing the pattern size to be below the typical crack spacing in continuous films, we further avoided the crack generation in the Si pattern. (Those cracks might consume irreversible lithium by forming SEI on the fresh fractured surfaces, leading to capacity degradation.) As a result, we were able to retain the good cycling stability without forming microcracks.

The fracture mode of continuous Si thin films during the lithation and delithation process differs from that of the patterned Si thin film. The fracture of the continuous film is due to the strain energy release rate exceeding the film's fracture strength. In contrast, the delamination of patterned Si should be due to the strain energy rate associated with interfacial fracture exceeding the interfacial strength between Si and Cu. However, in the latter case, the stress concentration around the edge may also lead to delamination before channeling cracks form in the large patterned Si thin films.

The size effect shown here is strongly dependent on the plastic zone present during cycling, which might reach several microns due to the emission and propagation of dislocations. One observation is the accumulating plastic deformation of the copper substrate during cycling because of the crack gaps becoming larger with increasing cycles [14]. We compared the modulus and hardness of the Cu substrates where Si peeled off after cycling with those of the uncoated regions, as shown in Fig. 8. The displacement showing in the figures stands for the penetration depth of the indentor. Both values increased in the top surface layer after the cycling, and the accumulation of dislocations in the top layer of the Cu substrate, which underwent plastic deformation, is believed to result in the hardness increase. At the same time, the hardening effect caused material pileup around the indent, leading to apparent increase of modulus during the measurement [18,19]. The plastic deformation of the Cu substrate during the cycling was also reported in [20]. The following section will provide some preliminary theoretical considerations for the unique fracture behaviors related to size and geometry of amorphous Si thin films on Cu substrates.

4. Theoretical considerations

The observed crack spacing in the Si thin film and critical patch size for Si delamination from Cu substrate cannot be straightforwardly explained by conventional theories of thin film fracture mechanics. Most of the existing theories on crack patterns in thin films or multilayers [21–28] predict crack spacing on the same order as the film thickness except when the Young's modulus of the film is much larger than that of the substrate [27,28]. This is generally consistent with experimental observations of crack patterns in engineering films/coatings [21–23,25] as well as crack spacing in rock layers [24]. Also, cracks in drying mud show an average spacing comparable to their depth [29], while crack patterns in drying cornstarch and cooling lava even have columnar structures with crack spacing much smaller than the depth [30]. In contrast to these theories and observations, our experiments showed that lithiated 100 nm thick Si films exhibited a mean crack spacing of 5–10 μm which is nearly two orders of magnitude larger than the film thickness. Since the Young's modulus of lithiated Si is actually smaller than that of Cu, this large difference between crack spacing and film thickness cannot be understood from the conventional theories of thin film fracture. Also, existing theories of edge crack delamination

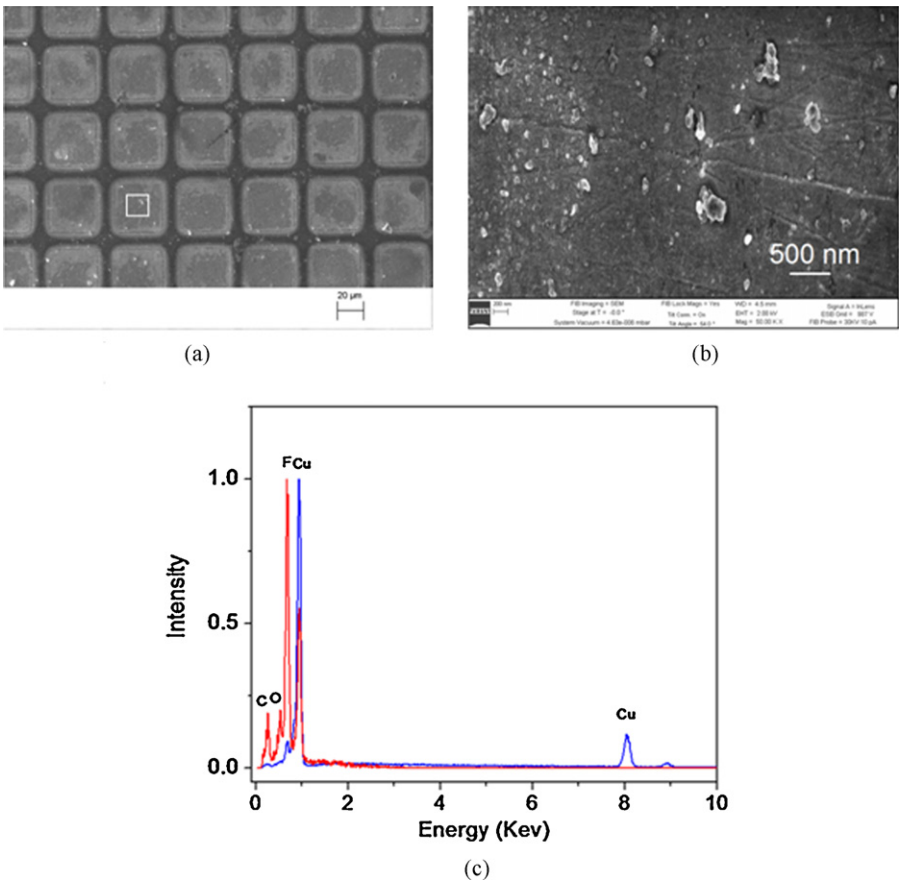

Fig. 5. Surface morphology and composition analysis of tested Si pattern made with 500 mesh mask. (a) SEM image after cycling. (b) High resolution image of surface morphology. (c) EDX analysis on patterned location. No Si signal was detected, indicating that Si patterns have delaminated.

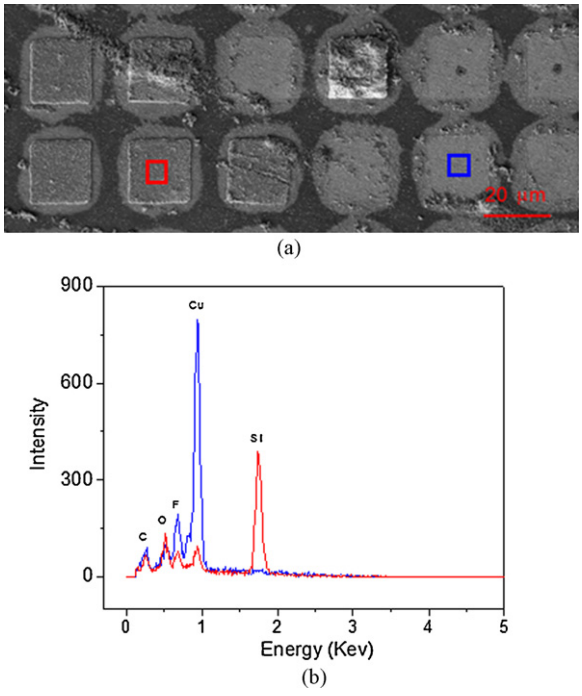

Fig. 6. Surface morphology and composition analysis of tested Si pattern made with 1000 mesh mask. (a) SEM image after cycling shows part of Si patterns has delaminated. (b) EDX analysis on patterned location. No Si signal was detected on the blue square, indicating that Si pattern has delaminated. In contrast, strong Si signal was detected on red square, indicating that Si pattern remained. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

[31] predict that the energy release rate associated with a delamination crack attains a steady-state value independent of the crack length as soon as the crack size becomes comparable to the film thickness. This implies that the size effect associated with Si patch delamination should arise only when the patch size is on the same order of its thickness. In contrast, our experiments demonstrate a strong size effect and drastically different delamination behaviors as the size of Si patches is reduced from 40 to 7 μm. This size scale is again two orders of magnitude larger than the film thickness (100 nm) and the observed size effect cannot be explained by conventional theories of thin film delamination.

We believe that the apparent discrepancies between the existing theories of thin film fracture/delimination and our present experimental observations are due to plastic deformation in both lithiated Si film and the Cu substrate. We note that Cu is known to yield at a tensile stress of about 70 MPa, and recent experiment [17] has shown that the lithiated Si film undergoes plastic flow as soon as the film stress reaches about $\sigma_Y^{Si} = 1 - 1.75$ Gpa.

The following questions are especially interesting: (1) What determines the crack spacing in Si film on Cu subtrate? (2) Why is the crack spacing in Si film also a measure of how large Si patches can stay on Cu substrates without delamination? What is the connection between Si thin film fracture and interfacial delamination of patterned Si patches?

To understand question (1), let us consider a Si film which already contained an array of cracks with spacing L (Fig. 9a). In this configuration, we ask if there exists a minimum crack spacing which would be so small that it does not allow an additional crack to be inserted in between the existing cracks. We assume this additional crack would form via plastic strain localization between two

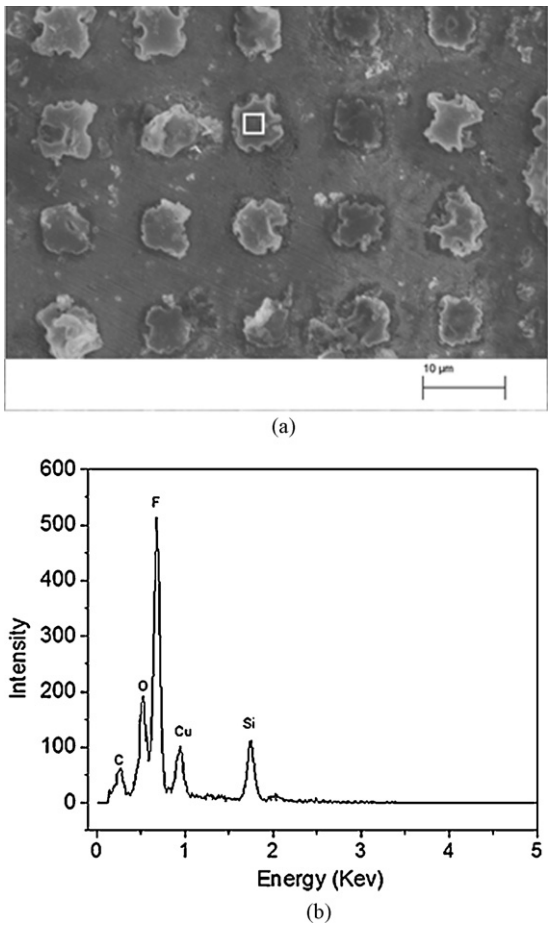

Fig. 7. Surface morphology and composition analysis of tested Si pattern made with 2000 mesh mask. (a) SEM surface morphology shows Si patterns remained on Cu substrate. (b) EDX detected Si on patterned region.

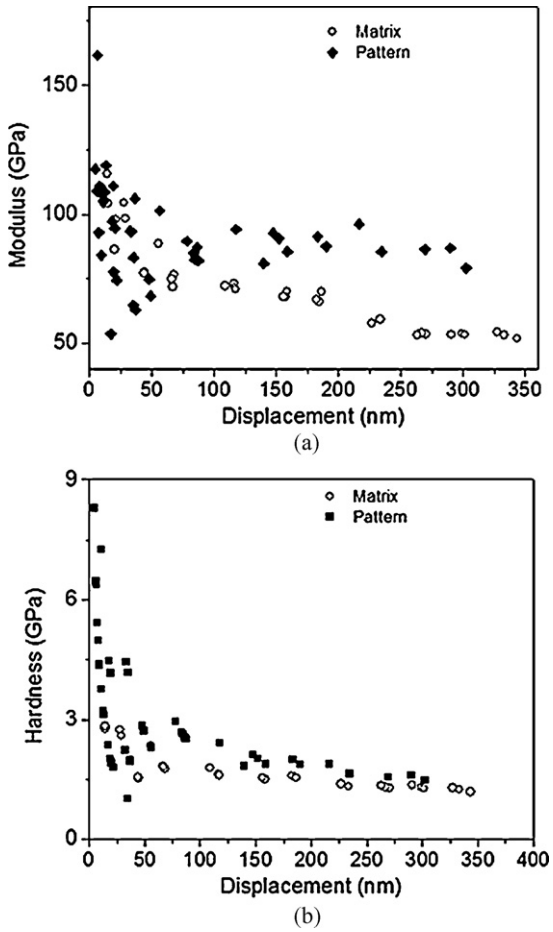

Fig. 8. Comparison of modulus (a) and hardness (b) of Cu substrate (Matrix) at the pattern location where Si has delaminated after cycling.

neighboring cracks in Si. Considering the free body diagram shown in Fig. 9b, force equilibrium in the critical configuration when the Si patch just begins to yield indicates

$$\frac{\tau_{cr}^{int} L_{cr}}{2} = \sigma_Y^{Si} h \tag{3}$$

where τ_{cr}^{int} is the interfacial shear strength between lithiated Si and Cu, which should be bounded by the shear flow stress of Cu and the interfacial friction strength, i.e.

$$\tau_{cr}^{int} = \min(\tau_Y^{Cu}, \tau_f^{int}) \tag{4}$$

Since the shear flow stress of Cu is about $\tau_Y^{Cu} = 40$ MPa and the apparent friction strength of metal–mica (Silicate composite) interface has been measured to be also around $\tau_f^{int} = 40$ MPa [32], a rough estimate of the interfacial shear strength between lithiated Si and Cu is thus $\tau_{cr}^{int} = 40$ MPa. Further, taking $h = 100$ nm and $\sigma_Y^{Si} = 1 - 1.75$ GPa immediately suggests that the minimum crack spacing preventing further plastic strain localization in Si film is

$$L_{cr} = \frac{2\sigma_Y^{Si}}{\tau_{cr}^{int}} h \sim 5.1 - 8.9\,\mu m \tag{5}$$

This length scale is in excellent agreement with the experimentally observed crack spacing in the 100 nm thick Si film. Below L_{cr}, plastic strain localization in Si becomes impossible because the stress in Si cannot reach the plastic flow stress of lithiated Si.

To understand why the crack spacing in Si film also determines the critical patch size for interfacial delamination, we note that dislocation activities in the Cu substrate (as shown Fig. 8) could induce

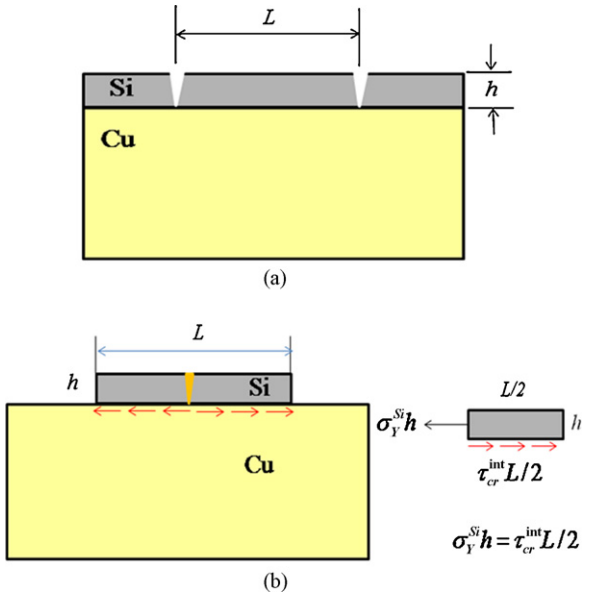

Fig. 9. Schematic of fracture in lithiated Si film on Cu substrate. (a) The configuration of a Si film with a periodic array of cracks of spacing L on Cu substrate. (b) The minimum crack spacing that could no longer allow an extra crack to be formed in between the existing cracks. Below this minimum crack spacing, the stress in the lithiated Si film could not reach its plastic yield stress and therefore no strain localization in the film can take place to form an additional crack.

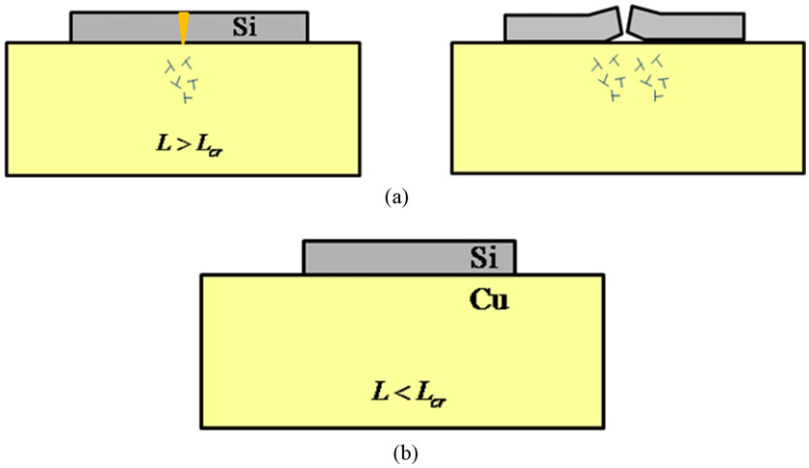

Fig. 10. Relationship between the critical crack spacing L_{cr} in the Si film and critical size of Si patches against interfacial delamination. (a) If the Si patch is larger than L_{cr}, the Si patch remains susceptible to plastic strain localization inside the patch. The localized deformation induces dislocation activities in the Cu substrate which, under cyclic lithiation and delithiation processes, induce interfacial delamination of lithiated Si film from Cu substrate. (b) If the Si patch is smaller than L_{cr}, no plastic strain localization within the Si patch is possible because the film stress is below the plastic flow stress of lithiated Si. In this case, dislocation activities in Cu are insufficient to cause interfacial delamination.

cyclic fatigue crack growth along the Si/Cu interface. Indeed, discrete dislocation (DD) simulations showed that dislocation induced cyclic fatigue crack growth could take place at stress levels well below those required for static crack growth [33]. We have performed DD simulations of interfacial delamination of periodic Si patches on Cu substrate and found that dislocation source density plays a critical role for the nucleation of a delamination crack [34]. Combining this important information from discrete dislocation simulations of Si delimination from Cu substrate and the concept of a minimum crack spacing in Si film, we hypothesize the following scenarios for the delamination of Si patches from Cu substrate (as shown in Fig. 10): Patterned Si patches with size well above L_{cr} remain susceptible to plastic strain localization in Si whose deformation then induce a large amount of dislocation activities in the Cu substrate which, under cyclic lithiation and delithiation processes, further induce interfacial delamination of lithiated Si film from Cu substrate. On the other hand, if the starting patch size is below L_{cr}, no plastic strain localization in Si is possible because the film stress will be below the plastic flow stress of lithiated Si, which then prevents a cascade of dislocation activities in Cu and in turn suppresses interfacial delamination. This sequence of events suggested by our length scale analysis and preliminary DD simulations provide a feasible explanation for our experimental observations. Our study indicates that the mechanical degradation of Si films/patches on Cu substrates depend strongly on coupled plastic deformation in both Si and Cu, which is distinct from most of the film/substrate systems studied in the literature. Much further theoretical and experimental studies will be needed to fully clarify the mechanisms involved.

5. Conclusions

The microcracks generated during cycling of a Si thin film electrode are typical channel-through cracks with an average crack spacing ranging from 7 to 10 μm. The designed Si patterns with a size below 7–10 μm remained adhered to the Cu substrate during the cycling test, leading to much better cycling stability and capacity retention. The gaps between Si patterns provide stress relaxation and better cycling stability relative to a continuous film. We have also provided some preliminary theoretical considerations about the correlation between crack spacing feature and different failure mechanisms between continuous film and patterned film. These results suggest a new approach to extend the cycle life of Si-based electrode materials using size to control and relax the stress due to lithiation and delithiation.

Acknowledgments

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